WHAT IS CLAIMED IS:

1. A semiconductor device having: a wiring substrate; a microcomputer chip; and a memory chip, said microcomputer chip and said memory chip being mounted over the upper surface of said wiring substrate,

wherein said microcomputer chip is constructed of a multiport structure including an interface between it and the inside of said system including said memory chip and an interface between it and the outside of said system, respectively,

wherein said memory chip is constructed so as to be accessed to the outside of said system via said microcomputer chip, and

wherein said microcomputer chip is mounted over said wiring substrate in a state being stacked over said memory chip.

2. The semiconductor device according to claim 1, wherein said microcomputer chip is connected to first electrodes of said wiring substrate via a plurality of bonding wires, said memory chip is connected to second electrodes of said wiring substrate via a plurality of bonding wires or a plurality of bump electrodes, and said first electrodes are arranged at the outer periphery side of said wiring substrate from said second electrodes.

3. The semiconductor device according to claim 1, wherein said memory chip is formed with a DRAM or a flash memory.

4. The semiconductor device according to claim 1, wherein said microcomputer chip is connected to first electrodes of said wiring substrate via a plurality of bonding wires, said memory chip is connected to second electrodes of said wiring substrate via a plurality of bonding wires, said first electrodes are arranged at the outer periphery side of said wiring substrate from said second electrodes, and the outer dimensions of said microcomputer chip are equal to or larger than those of said memory chip.

5. The semiconductor device according to claim 4, wherein a spacer is interposed between said microcomputer chip and said memory chip.

6. A semiconductor device having a System in Package structure in which a system is constituted of: a wiring substrate; one microcomputer chip; and two memory chips, said microcomputer and said memory chips being mounted over the upper surface of said wiring substrate,

wherein said microcomputer chip is constructed of a multiport structure including an interface between it and the inside of said system including said two memory chips and an interface between it and the outside of said system, respectively,

wherein each of said two memory chips is constructed so as to be accessed to the outside of said system via said microcomputer chip, and

wherein said two memory chips are mounted over said wiring substrate in a state that one of them is stacked over the other and said microcomputer chip is mounted over said wiring substrate in a state of being stacked over said two memory chips.

7. The semiconductor device according to claim 6, wherein said microcomputer chip is connected to first electrodes of said wiring substrate via a plurality of bonding wires, the memory chip as the lower layer of said two memory chips is connected to second electrodes of said wiring substrate via a plurality of bump electrodes, the memory chip as the upper layer thereof is connected to third electrodes of said wiring substrate via a plurality of bonding wires, and said first electrodes are arranged at the outer periphery side of said wiring substrate from said second and third electrodes.

8. The semiconductor device according to claim 6, wherein one of said two memory chips is formed with a DRAM, and the other is formed with a flash memory.

9. The semiconductor device according to claim 6, wherein the lower surface of said wiring substrate is formed with a plurality of bump electrodes constructing external connection terminals.